DA and AD Converters in SiGe Technology: Speed and Resolution for Ultra High Data Rate Applications

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Abstract DA and AD converters are key elements for implementing new modulation formats in next generation optical transport systems. Latest results and future trends are presented with a focus on SiGe devices.

Introduction
Using AD and DA converters on either the RX or TX side of a transmission system will open up new qualities in robustness and efficiency of optical transmission systems. For most of the currently investigated 100 GbE systems, binary modulation formats in combination with polarization multiplexing is used. In this case there is (apart from preemphasis) no need for a DA converter at the TX side. On RX side, although transmission is binary, ADCs are increasingly used, since they allow for more complex and flexible digital equalization and compensation using a DSP.

When targeting higher bit rates per wavelength, while keeping 50 GHz optical channel spacing, equalization and compensation using a DSP. allows for more complex and flexible digital equalization and compensation using a DSP.

Technolog Choice
Some state-of-the-art converters are listed in Tab. 1. While CMOS announces record sampling rates for AD converters, DA converters with high sampling rates are a SiGe domain. The main reason why CMOS performs well at ADCs only is that the key element for high sampling rates in ADCs is the track and hold (T/H). Once a fast T/H is available, the signal can be further down-sampled and processed by interleaved ADC cores, e.g. 320 SAR (successive approximation register) ADCs. In this case, the limiting factor is the signal and clock distribution up to the first set of T/H elements. This is where SiGe has major advantages with respect to bandwidth and gain, which makes even the integration of (in real systems required) AGC and TIA amplifiers possible.

Regarding DACs, things look a little bit different. DACs cannot be easily interleaved, since switching noise of the interleaver (practically an analog multiplexer) is visible at the output. In addition, measures to avoid pattern effects in the output stage become difficult in case of interleaving. Nevertheless, there are some investigations using interleaving for DACs in CMOS.

Looking at SiGe bipolar devices, the excellent transistor transconductance allows for direct connection of the output of the DA stage, combining high bandwidth and low rise/fall time with reasonable

![Table 1: Some state-of-the-art converter results](image)

Sampling Rate (SR); Phys. resolution (Res); 20%-80% rise/fall-time (t); full-scale swing (V); effective number of bits (ENOB) at f=f<sub>ENOB</sub>; Power dissipation (P); Literature (Ref)erence.
swing. Currently, 1.6 Vpp, diff are reached, with the target to drive Mach-Zehnder and EAM modulators directly in future. One of the main driving factors for implementation of the converter on the same chip as the DSP is the massive data bus which e.g. needs to transfer 180 Gb/s for 30 GS/s and 6 bit resolution. On the other hand, using separate chips for converter and DSP allows for choosing the best technology node for each device. Since new CMOS technologies are usually optimized for logic gates first, this two chip approach enables rapid transfer to latest technologies for the DSP or FPGA, while keeping the utmost speed/bandwidth in the SiGe core. In this case, 3D mounting technologies with through silicon vias are viable solutions for energy efficient interconnects between SiGe and CMOS devices. Furthermore, while specially designed DSPs are the best choice with respect to energy efficiency, FPGA based solutions enable multi-format transmitters and more flexibility, e.g. changing formats “on-the-fly”. Therefore, Micram develops DA and AD converters in SiGe bipolar, which can either be used in a two chip approach (together with a CMOS DSP/FPGA) or carry “smaller” amount of logic in case of BiCMOS. In the next couple of sections these converters are discussed in more detail.

**Digital to Analog Converter**

The most critical building block of the DAC is the converter core, which takes the digital words at full speed and converts them to analog voltages. For best signal integrity a single core output is used, which sums weighted currents at load resistors. In ADCs commonly used interleaving of converter cores is difficult for DACs, since it requires a highly linear analog multiplexer. This is sensitive to pattern effects (e.g. due to self heating) and introduces switching noise.

Typical digital to analog converter structures used in high-speed converters are R2R ladders and summing weighted currents. R2R ladders are challenging especially at high frequencies with respect to impedance matching and timing. Instead, an approach with binary weighted current switches was chosen. The currents are summed in a common node (Fig. 1), simplifying routing and improving timing control. The remaining timing problem is due to the current ratio between the stages (1:32 for 6 bit). To get the maximum speed, the switching transistors need to be operated at identical current densities, which are typically chosen for maximum $f_T$. This results in very small transistors for the LSB, while the MSB uses multiple large transistors in parallel. Accurate timing optimization in the interaction between the latches and the output driver switches is necessary at this point. An adequate impedance matching is used to drive both, the internal 50 ohm termination as well as the external 50 ohm load.

![Image of DA converter with binary weighted current switches.](image)

**Fig. 1:** DA converter with binary weighted current switches.

This architecture is likely to show glitches, especially at the most significant bit (MSB) transition 6'b011111 to 6'b100000. In this case, the absolute value changes only one LSB, but all current switches need to alternate. Fig. 2 shows the center of a 64 steps ramp, measured at 25 GSa/s. Glitches at the MSB switching as well as at MSB-1 and MSB-2 are clearly visible. To reduce these glitches, a decoder was introduced in a more advanced approach. The three most significant bits are decoded from binary values of D[5:3] to thermometer code K[6:0], as shown in Fig. 3. Of course this adds some additional logic gates to the circuit (no additional current is required in the output driver), but reduces the glitches drastically. Fig. 4 shows again a 64 step ramp for this improved output stage, where the glitches have nearly disappeared.

![Image of output ramp of DAC core as shown in Fig. 1.](image)

**Fig. 2:** Output ramp of DAC core as shown in Fig. 1. introduced in a more advanced approach. The three most significant bits are decoded from binary values of D[5:3] to thermometer code K[6:0], as shown in Fig. 3. Of course this adds some additional logic gates to the circuit (no additional current is required in the output driver), but reduces the glitches drastically. Fig. 4 shows again a 64 step ramp for this improved output stage, where the glitches have nearly disappeared.
DAC Measurement results

The measurements presented here are derived from the most recent Vega DA converter series (DAC30). All measurements were performed using the set-up described later in the section “Measurement setup”.

Tab. 2 lists some key data of the DAC30 device. This device includes the DAC core as well as lots of additional circuits to connect to a standard FPGA for real time processing. The device is designed to operate over a wide range from dc to 34 GSa/s. Most of the power consumption (70%) is due to the FPGA interface and the wide band clock distribution. The high-speed DAC core consumes only 0.4 W without and 3.7 W with the multiplexers and decoders. The integral nonlinearity (Fig. 5) is better than 0.2 LSB, which indicates that there is room for increasing the bit count and therefore at least the dc resolution.

The full scale output swing can be adjusted in a wide range of 400...1600 mVpp by changing (serial register programming) the reference current $. The output amplitudes up to 1900 mVpp are possible with minor degradation in RF performance due to transistor saturation. In addition, the current sources can be fine tuned for optimum INL.

Another typical key value is the effective number of bits (ENOB), which can be determined in the frequency domain. When speaking of ultra high data rates, the ENOB value is hardly to measure and not comprehensive. For example, at 28 GSa/s and beyond, we see an overlay of circuit imperfections as well as assembly and interfacing imperfections (cf. section “Outlook”).

Tab. 2: DAC30 key data.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling rate</td>
<td>dc – 34 GSa/s</td>
</tr>
<tr>
<td>Resolution</td>
<td>6 bit</td>
</tr>
<tr>
<td>Rise/Fall (20/80%)</td>
<td>12 ps</td>
</tr>
<tr>
<td>INL</td>
<td>$&lt; 0.2$ LSB</td>
</tr>
<tr>
<td>Full scale swing</td>
<td>800 mV,se</td>
</tr>
<tr>
<td></td>
<td>1600 mV,pp</td>
</tr>
<tr>
<td>ENOB*</td>
<td>5.27</td>
</tr>
<tr>
<td>SFDR*</td>
<td>46.9 dB</td>
</tr>
<tr>
<td>Total power diss.</td>
<td>12.5 W</td>
</tr>
<tr>
<td>Converter core power</td>
<td>0.4 W</td>
</tr>
<tr>
<td>Die size</td>
<td>5.07 x 5.07 mm²</td>
</tr>
<tr>
<td>Converter core size</td>
<td>0.40 x 0.43 mm²</td>
</tr>
<tr>
<td>DA core incl. last mux/FF</td>
<td>0.80 x 1.30 mm²</td>
</tr>
</tbody>
</table>

(*28 GSa/s, 875 MHz sine wave output, measured with spectrum analyser up to Nyquist frequency)

Fig. 3: DA converter with decoding of three most significant bits.

Fig. 4: Output ramp of DAC core with decoding of MSBs.

Fig. 5: Integral nonlinearity of the DAC30.

Fig. 6: 16-step ramp at 28 GSa/s.
overall performance. It should be mentioned that the rise/fall time should be adjusted to the application, since DA converters for multi-level formats are expected to show clear open eye diagrams and therefore require steep edges. On the other hand, OFDM signals require only a bandwidth up to the Nyquist frequency. However, their very high time-domain dynamics require utmost pulse settling fidelity for any step height and direction.

**Analog to Digital Converter**

The key to high speed AD converters in SiGe is not to use massive parallelizing but fast ADC cores. A traditional concept for this is flash conversion. Flash converters are known for the fastest conversion speeds per core, but suffer from the number of parallel comparators, which need to be driven by the input signal (and the sampling clock), especially at higher resolutions, since the complexity increases by the power of two for each additional bit. Using an interpolating/folding architecture in the flash converter would reduce the amount of comparators by the factor of typically two.

For SiGe devices another concept is promising, the serial ripple converter. Although it is not as fast as a flash converter, it offers reasonable speed and has the great benefit of direct conversion to gray coded output (Fig. 7). This makes the logic required for flash converters obsolete. The gray code can be easily converted to binary either in the ADC or DSP/FPGA. Adding another bit of resolution only adds another amplifier and flip-flop stage to the chain. In the ADC30, four of those converters are interleaved. Each ADC has its own T/H buffer in front, operating 25% of the time in track mode and the remaining 75% in hold mode. The input stage was optimized to have a high sensitivity and bandwidth margin well beyond the first Nyquist band to demonstrate the performance which can be reached by increasing the interleave ratio.

**ADC Measurement Results**

Some key data of Micram’s current AD converter (ADC30) are listed in Tab. 3. Similar to the DAC30, a variable sampling rate from dc up to 34 GSa/s was targeted. Also, an FPGA

<table>
<thead>
<tr>
<th>Tab. 3: ADC30 key data.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sampling rate</strong></td>
</tr>
<tr>
<td><strong>Resolution</strong></td>
</tr>
<tr>
<td><strong>Full scale input range</strong></td>
</tr>
<tr>
<td><strong>INL</strong></td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
</tr>
<tr>
<td><strong>ENOB (30 GSa/s)</strong></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td><strong>Total power diss.</strong></td>
</tr>
<tr>
<td><strong>Converter core power</strong></td>
</tr>
<tr>
<td><strong>Die size</strong></td>
</tr>
<tr>
<td><strong>Converter size</strong></td>
</tr>
</tbody>
</table>

(*) second Nyquist band

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**Fig. 7:** Simplified principle of a serial ripple AD converter.

**Fig. 8:** Sinus fit (IEEE-STD-1241) of 25 GHz sine wave to 30 Gsa/s sampled data.
can be directly connected to the ADC30 for real time data processing. When using the internal 16-sample memory, an ENOB of 3.3 is achieved for a 25 GHz sine wave input at 30 GSa/s, i.e. the signal resides in the second Nyquist band (Fig. 8). The FPGA interface is currently limited to 10 GSa/s (being fixed in the next revision), showing similar results on 512 kS real time data.

FPGA Interface

Ideally, the interface to the signal processing (DSP or FPGA) should be source synchronous, i.e. there is no need for alignment and synchronization at all.

To enable stand-alone operating, an interface to currently available FPGAs was implemented in the Vega AD and DA converters. Common FPGA currently offer SerDes ports up to 6.6/8.5 Gb/s (and 11.18/11.3 Gb/s)\(^{23,24}\), while rates up to 28 Gb/s are targeted for new chip-to-chip and chip-to-module interfaces\(^{24}\). For the DAC/ADC devices the intention was to rely on an already existing SerDes interface. Therefore a times-4 multiplexed interface was chosen, which results in 7.5 Gb/s per line for 30 GSa/s operation. At 6-bit resolution, 24 serial lines are required. Data transfer is raw, since data encoding reduces the data net rate. For example, the commonly used 8b/10b encoding would add 25% overhead, which results in 5.2 Gb/s net data rate (i.e. 20.8 GSa/s) for a Virtex device at the nominal 6.5 Gb/s. Except for the required power consumption and wiring effort (which is tolerable for demonstrator setups), the transceivers in common FPGAs have some drawbacks:

1. The phase of each TX channel is random.
2. The transmitters show an initial reset dependent bit skew, varying at each start.
3. The phase of a TX channel changes over temperature.
4. The receiver CDRs need data traffic (transitions) to stay locked.
5. The received data of all channels need to be aligned.

When coupling to a DAC, the FPGA constraints 1-3 are of main interest. To compensate for (1), each channel’s phase can be programmed in 90° steps, instead of implementing a CDR. A CDR without framing would have the problem that one false decision destroys synchronisation. By using an initial synchronisation sequence, the bit skew (2) is compensated for. These measures also work for cable length mismatches.

Temperature drift (3) can be reduced by measuring the phase of the channels (built-in phase detectors) and shifting the reference clock accordingly.

In case of the ADC, the FPGA acts as a receiver. The CDR in the FPGA is always active, requiring sufficient transitions (4). Therefore, the data can be PRBS scrambled on the ADC. This also makes ac coupling possible. In addition, an initialization sequence can be sent by the ADC to align all channels (5).

Measurement setup

All measurements presented in this paper were performed with the chips mounted (wire-bond) in modules (Fig. 9). The clock and the analog DAC/ADC signal are fed directly to the module through K-connectors, while all other signals including the FPGA serial lines are carried to an evaluation board via mezzanine connectors. For the FPGA a Virtex4 board is used. The test setup including the FPGA is shown in Fig. 10. The ADC and the DAC chip both fit in the same module and use the same evaluation board. During tests, the DAC/ADC is clocked by a synthesizer, while the FPGA reference clocks for the SerDes transceivers are generated by the DAC/ADC.

Outlook: Beyond 100 GbE

The next step on the development road map will be 400 GbE, with data rates up to 448 Gb/s including FEC. These systems need higher
order modulation formats, and therefore definitely DA converters at the transmitter. Tab. 4 lists some requirements for the DAC as well as for the ADC.

In principle, the minimum effective DAC resolution can be directly derived from the required levels, while the required sampling rate is equal to the line rate in Gbaud. When using pre-distortion, oversampling may be required. Adding more bits to the DAC makes sense also in case of oversampling and compensating for e.g. non-linearities of modulators. OFDM also needs more bits and a high dynamic range of the DAC. Compensation for temperature/aging effects may require a low-speed DAC overlaid to the high-speed part.

For the ADC, usually a twofold oversampling is required to omit clock recovery circuits. Equalization at the receiver requires the ADC to have more bits than the signal originally uses. If there is no AGC at the input, the ADC will usually not always be driven by a full scale signal. This also requires some margin in the resolution.

Finally, it should be mentioned that it is challenging to maintain the high frequency performance and effective resolution throughout the passive components (traces, cables, connectors, package, etc.).

Taking a simple model with the reflection coefficients \( r_1 \) and \( r_2 \) on both ends, the requirement to keep double reflection below 1 LSB for a resolution of \( b \) bits is:

\[
|r_1| \cdot |r_2| \leq \frac{1}{2^b}.
\]

Written in dB, this equals to:

\[
\frac{r_1}{\text{dB}} \leq -b \cdot 6.02 - \frac{r_2}{\text{dB}}.
\]

For an 8-bit resolution, and the simple case of \( |r_1| = |r_2| \), this results in the requirement of a return loss of better than \( \approx 24 \) dB over the whole bandwidth on both ends of the transmission line.

**Conclusion**

Especially when looking at next generation 400 GbE, the transmission formats require for both extremely fast AD and DA converters. In general, there is a trade-off between sampling speed and resolution. Using SiGe devices is a viable way to serve the bandwidth and slew rate requirements for DA as well as for AD converters. Integration of TIA/AGC on the ADC will be an energy and cost efficient step in the future when using SiGe.

**Acknowledgement**

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**Tab. 4: ADC/DAC Requirements for 400 GbE**

<table>
<thead>
<tr>
<th>Bandwidth (GHz)</th>
<th>4-QAM</th>
<th>16-QAM</th>
<th>64-QAM</th>
<th>256-QAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC ENOB</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>ADC ENOB</td>
<td>3.8</td>
<td>4.9</td>
<td>5.7</td>
<td>7.0</td>
</tr>
</tbody>
</table>

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